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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/789,646 | 03/01/2004 | Muthiah Venkateswaran | 34105.1 | 9162 |

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| EXAMINER | |
|---|---|
| DOLAN, JENNIFER M | |
| **ART UNIT** | **PAPER NUMBER** |
| 2813 | |

DATE MAILED: 07/20/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/789,646 | VENKATESWARAN, MUTHIAH | |
| | Examiner | Art Unit | |
| | Jennifer M. Dolan | 2813 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *01 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *20-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *20-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/1/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 102*

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 20-22 and 25 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,521,530 to Peters (cited by applicant).

Regarding claim 20, Peters discloses a semiconductor device, comprising: a package substrate (900, 1000, 1400, etc.; see figures 7-16) having a top layer (layer upon substrate in figures 7 or 8; alternatively, the top portion of the substrate in figures 9-11 or 13), the top layer having a group of conductive vias (figures 7-16; see column 10, lines 1-20, lines 47-65; etc) formed therethrough; a layer of conductive material formed on the top layer of the package substrate (see figure 8g; 9c-d, 10c, 13c); a group of channels formed in the conductive material layer about at least some of the vias to define a group of contact pads on the vias (see figures 9d; 10d, 13d, and 16; column 10, lines 57-65); and a chip (see figure 14) electrically coupled to the package substrate through the contact pads.

Regarding claims 21 and 22, Peters discloses a copper conductive layer and copper-filled vias (column 12, lines 19-34).

Regarding claim 25, Peters discloses solder balls soldered on at least some of the contact pads, wherein the chip is electrically coupled to the package substrate via the solder balls (figure 14).

3. Claims 20-22 and 25 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,388,207 to Figueroa et al.

Regarding claim 20, Figueroa discloses a device comprising: a package substrate (71-73) having a top layer (71), the top layer having a group of conductive vias (76) formed therethrough (figure 4); a layer of conductive material (74) formed on the top layer of the package substrate (figure 4); a group of channels (gaps separating conductive layer 74 in figure 4) formed in the conductive layer about at least some of the vias to define a group of contact pads on the vias (figures 3-4); and a chip (50) electrically connected to the package substrate through the contact pads (figures 3-4).

Regarding claims 21 and 22, Figueroa discloses that the conductive layer and the conductive vias are made using copper (column 2, lines 5-11; column 7, lines 1-5; 19-24).

Regarding claim 25, Figueroa discloses solder balls (56) soldered to the contact pads, wherein the chip is connected to the pads on the package substrate via the solder balls (figures 3-4; column 5, lines 15-27).

4. Claims 20, 21, and 25 are rejected under 35 U.S.C. 102(a) as being anticipated by the Applicant's admitted prior art (hereforth AAPA).

Regarding claim 20, the AAPA discloses a semiconductor device comprising: a package substrate (see figure 1) having a top layer (42), the top layer having a group of conductive vias (36) formed therethrough (figures 1-6); a layer of conductive material (40) formed on the top layer of the package substrate (figure 2); a group of channels (figure 3; spaces between pads 44) formed in the conductive material layer about at least some of the vias to define a group of contact pads (44; see figure 3 and Applicant's specification, paragraph 0003); and a chip (52) electrically coupled to the package substrate (figure 6).

Regarding claim 21, the AAPA teaches that the conductive layer is made of copper (paragraph 0003).

Regarding claim 25, the AAPA discloses solder balls (50) soldered on at least some of the contact pads, wherein the chip is electrically coupled to the pads via the solder balls (figure 6; paragraph 0004).

***Claim Rejections - 35 USC § 103***

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 23 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Peters et al. in view of U.S. Patent No. 6,312,974 to Wu et al.

Regarding claim 23, Peters fails to disclose an oxide layer formed over the conductive layer.

Wu teaches a package substrate (see figures 2-4) having contact pads (56, 92), wherein an oxide layer (58 or 94) is formed over the conductive pad layer, with portions of the oxide layer removed on at least some of the contact pads (see figures 2c-2d; 3d; also see column 7, lines 35-50; column 8, lines 15-27).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the structure of Peters, such that the surface oxide layer is provided, as taught by Wu. The rationale is as follows: A person having ordinary skill in the art would have been motivated to provide a surface oxide layer overlying the contact layer but having openings over the contact pads, because an oxide layer would provide insulation between the package substrate and the overlying chip, it would restrain and direct the solder for making an interconnection, and it would provide protection and passivation for the package substrate, as is appreciated by a person having ordinary skill in the art (also see Wu, column 8, lines 15-27).

Regarding claim 24, Peters discloses solder balls soldered on at least some of the contact pads, wherein the chip is electrically coupled to the package substrate via the solder balls (figure 14).

7. Claims 23 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Figueroa in view of Wu.

Regarding claim 23, Figueroa fails to disclose an oxide layer formed over the conductive layer.

Wu teaches a package substrate (see figures 2-4) having contact pads (56, 92), wherein an oxide layer (58 or 94) is formed over the conductive pad layer, with portions of the oxide layer

removed on at least some of the contact pads (see figures 2c-2d; 3d; also see column 7, lines 35-50; column 8, lines 15-27).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the structure of Figueroa, such that the surface oxide layer is provided, as taught by Wu. The rationale is as follows: A person having ordinary skill in the art would have been motivated to provide a surface oxide layer overlying the contact layer but having openings over the contact pads, because an oxide layer would provide insulation between the package substrate and the overlying chip, it would restrain and direct the solder for making an interconnection, and it would provide protection and passivation for the package substrate, as is appreciated by a person having ordinary skill in the art (also see Wu, column 8, lines 15-27).

Regarding claim 24, Figueroa discloses solder balls (56) soldered to the contact pads, wherein the chip is connected to the pads on the package substrate via the solder balls (figures 3-4; column 5, lines 15-27).

***Conclusion***

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. U.S. Patent No. 6,800,947 to Sathe discloses a package substrate having narrow channels separating the upper surface contact pads.

b. U.S. Patent No. 6,828,669 to Iijima et al. discloses a package substrate wherein a contact pad is exposed on the top surface, but has resin material applied to the side surfaces.

c. U.S. Patent Publication No. 2003/0122213 to Hsu et al. discloses a package substrate structure having the claimed vias, contact pads, and a solder mask disposed on the conductive contact pad layer.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jennifer M. Dolan whose telephone number is (571) 272-1690. The examiner can normally be reached on Monday-Friday 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl W. Whitehead, Jr. can be reached on (571) 272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jennifer M. Dolan
Examiner
Art Unit 2813

jmd

CARL WHITEHEAD JR.
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800